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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,803	01/26/2004	Payman Zarkesh-Ha	02-5938	9749
24319	7590	08/06/2007	EXAMINER	
LSI CORPORATION			KIM, SU C	
1621 BARBER LANE				
MS: D-106			ART UNIT	PAPER NUMBER
MILPITAS, CA 95035			2823	
			MAIL DATE	DELIVERY MODE
			08/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/764,803	ZARKESH-HA ET AL.
Examiner	Art Unit	
Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 April 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-24 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 26 January 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. _____.
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____ 5) Notice of Informal Patent Application
 _____ 6) Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Applicant Argument pages 9-10, filed 4/30/2007, with respect to claims 1-24 have been fully considered and are persuasive. The rejections of claims 1-24 have been withdrawn.

Claim Rejections - 35 USC § 112

2. Claims 1, 18, 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is confusing to recite "field programmable platform array".

Is it field programmable gate array? Memory?

The examiner considers "field programmable platform array" as any field programmable array such as memory, field programmable gate array, any semiconductor device with programmable function.

In claim 18, & 20-23, it is confusing to recite "a routing layer" because the examiner can not define that a routing layer is directing an additional routing layer or pre-routing metal layer?

The examiner considers "a routing layer" as any interconnection between a semiconductor device.

Claim 18 recites the limitation "top aluminum pads" in claim 18. There is insufficient antecedent basis for this limitation in the claim.

Since the claim language renders indefinite, as stated in the rejection under U.S.C 112, second paragraph, the rejection made in this Office Action is based on the best understanding of the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

((b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-13, & 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Or-bach (US 2001/0038297)

Regarding claims 1, 9, & 17, Or-Bach discloses a method for providing field programmable platform array units, comprising:

cutting N by M array of platform array units from a field programmable platform array wafer according to an order from a customer , N and M being positive integers (Fig. 61), said field programmable platform array (paragraph 0606) wafer having all silicon layers (paragraph 0587) and metal layers (paragraph 0592)already built and including a plurality of platform array units (Fig. 45B) , said plurality of platform array units being field programmable by a customer (paragraph 0622), each of said plurality of platform array units including at least one core and at least one processor (Fig. 57), and interconnect between said plurality of platform array units being pre-routed on chip

(Fig. 57); and packaging and testing (paragraph 0104) said N by M array of platform array units.

Regarding claims 2 & 10, as applied to claims 1 & 10, Or-bach discloses all the limitations including, programming said N by M array of platform array units by said customer (paragraph 0134).

Regarding claims 3 & 11, as applied to claims 2 & 10, Or-bach discloses all the limitations including, said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications (Fig. 57, paragraph 0571)).

Regarding claims 4 & 12, as applied to claims 2 & 10, Or-bach discloses all the limitations including, said programming is performed with firmware (paragraph 0031 & 0571, note: design compiler).

Regarding claims 5 & 13, as applied to claims 1 & 9, Or-bach discloses all the limitations including, said N by M array of platform array units are within a single platform (Fig. 57).

Regarding claims 7 & 15, as applied to claims 5 & 13, wherein said single platform is a digital signal processing (DSP) platform (paragraph 00597).

Regarding claims 8 & 16, as applied to claims 1 & 9, Or-bach discloses all the limitations including, storing said field programmable platform array wafer 4012 (Fig. 57, note: data MEM)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Or-bach (US 20010038297) in view of Mastro et al. (US 20020091977)

Regarding claims 6 & 14, as applied to claims 5 & 13, Or-bach discloses all the limitations including, said single platform.

Or-bach fails to teach said single platform is a storage area network (SAN) platform.

However, Mastro suggests said single platform 94 (Fig. 5, FPGA) is a storage area network (paragraph 0067).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Or-bach reference with said single platform is a storage area network (SAN) platform as taught by Mastro in order to enhance functionality.

7. Claims 18 & 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Or-bach (US 20010038297) in view of Lee et al. (US 6222212)

Regarding claims 18 & 20-23, as applied to claim 17, Or-bach discloses all the limitations including, said semiconductor device are used as a routing layer (Fig. 57) Or-bach fails to teach a routing layer (interconnection) is made of one material from a group comprising aluminum, copper, or polysilicon.

However, Lee discloses the routing layer can be made of aluminum, copper, polycrystalline silicon (column 5, lines 30-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Or-bach reference with a routing layer (interconnection) is made of one material from a group comprising aluminum, copper, or polysilicon as taught by Lee in order to enhance electrical conductivity.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Or-bach (US 2001/0038297) in view of Lee et al. (US 6,222,212) and further in view of Huang et al. (US 6,396,129)

Regarding claim 19, as applied to claim 18, Or-bach and Lee in combination disclose all the limitations including, said semiconductor device.

However, Or-bach and Lee in combination fail to teach encapsulation of lower metal layers of said semiconductor device.

Huang discloses encapsulation 150 of metal layer (Fig. 3C, column 4, lines 20-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide A reference with encapsulation of lower metal layers of said semiconductor device as taught by Huang in order to enhance bonding strength.

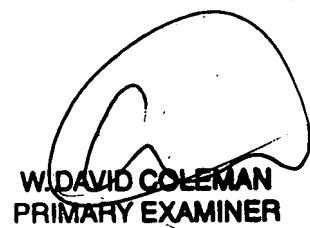
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Su C Kim



W. DAVID COLEMAN
PRIMARY EXAMINER